ATME COLLEGE OF ENGINEERING

MYSURU-570028

VLSI Design

NOTES FOR 6TH SEMESTER
ELECTRONICS & COMMUNICATION ENGINERRING

SUBJECT CODE : BEC602

INSTITUTIONAL MISSION AND VISION

Vision

- Development of academically excellent, culturally vibrant, socially responsible and globally competent human resources.

Mission

- To keep pace with advancements in knowledge and make the students competitive and capable at the global level.
- To create an environment for the students to acquire the right physical, intellectual, emotional and moral foundations and shine as torch bearers of tomorrow's society.
- To strive to attain ever-higher benchmarks of educational excellence.

DEPARTMENTAL MISSION AND VISION

Vision

To develop highly skilled and globally competent professionals in the field of Electronics and Communication Engineering to meet industrial and social requirements with ethical responsibility.

Mission

- To provide State-of-art technical education in Electronics and Communication at undergraduate and post-graduate levels, to meet the needs of the profession and society and achieve excellence in teaching-learning and research.
- To develop talented and committed human resource, by providing an opportunity for innovation, creativity and entrepreneurial leadership with high standards of professional ethics, transparency and accountability.
- To function collaboratively with technical Institutes/Universities/Industries, offer opportunities for interaction among faculty-students and promote networking with alumni, industries and other stake-holders.
- To provide State-of-art technical education in Electronics and Communication at undergraduate and post-graduate levels to meet the needs of the profession and society.

Program outcomes (POs)

Engineering Graduates will be able to:

PO1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO5. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO5. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSOs)

At the end of graduation the student will be able,

- To comprehend the fundamental ideas in Electronics and Communication Engineering and apply them to identify, formulate and effectively solve complex engineering problems using latest tools and techniques.
- To work successfully as an individual pioneer, team member and as a leader in assorted groups, having the capacity to grasp any requirement and compose viable solutions.
- To be articulate, write cogent reports and make proficient presentations while yearning for continuous self-improvement.
- To exhibit honesty, integrity and conduct oneself responsibly, ethically and legally; holding the safety and welfare of the society paramount.

Program Educational Objectives (PEOs)

- Graduates will have a successful professional career and will be able to pursue higher education and research globally in the field of Electronics and Communication Engineering thereby engaging in lifelong learning.
- Graduates will be able to analyze, design and create innovative products by adapting to the current and emerging technologies while developing a conscience for environmental/ societal impact.
- Graduates with strong character backed with professional attitude and ethical values will have the ability to work as a member and as a leader in a team.
- Graduates with effective communication skills and multidisciplinary approach will be able to redefine problems beyond boundaries and develop solutions to complex problems of today’s society.

MODULE 1 Basic MOS Technology

Transistor was first invented by William.B.Shockley, Walter Brattain and John Bardeen of Bell Labratories. In 1961, first IC was introduced.

Levels of Integration:-

i) SSI:- (10-100) transistors => Example: Logic gates
ii) MSI:- (100-1000) => Example: counters
iii) LSI:- (1000-20000) => Example:8-bit chip
iv) VLSI:- (20000-1000000) => Example:16 & 32 bit up
v) ULSI:- (1000000-10000000) => Example: Special processors, virtual reality machines, smart sensors

Moore's Law:- "The number of transistors embedded on the chip doubles after every one and a half years." The number of transistors is taken on the y-axis and the years in taken on the x- axis. The diagram also shows the speed in MHz. the graph given in figure also shows the variation of speed of the chip in MHz

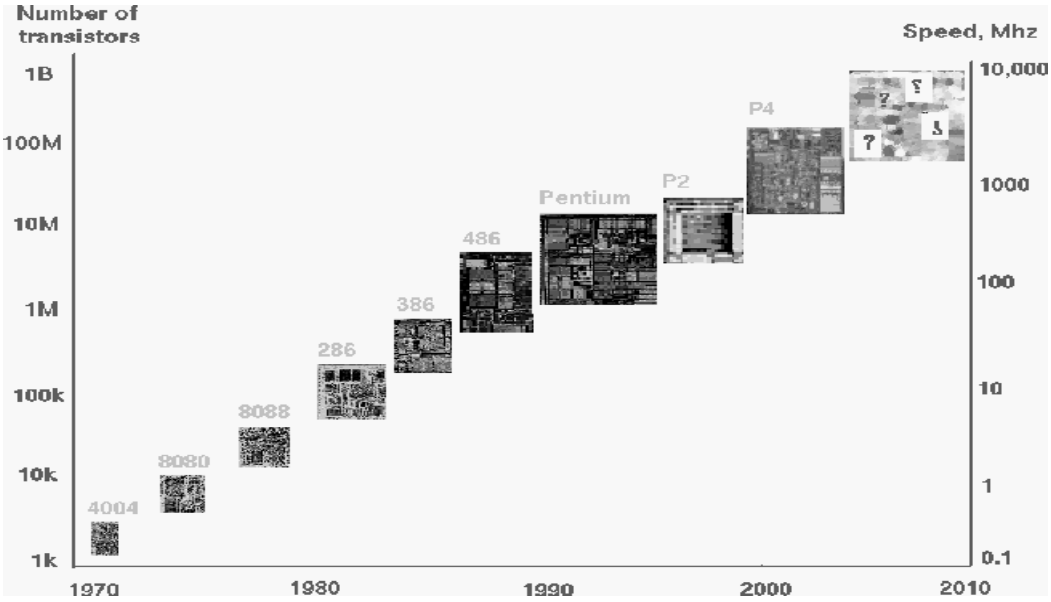


Figure 1. Moore's law

The graph in figure2 compares the various technologies available in ICs.

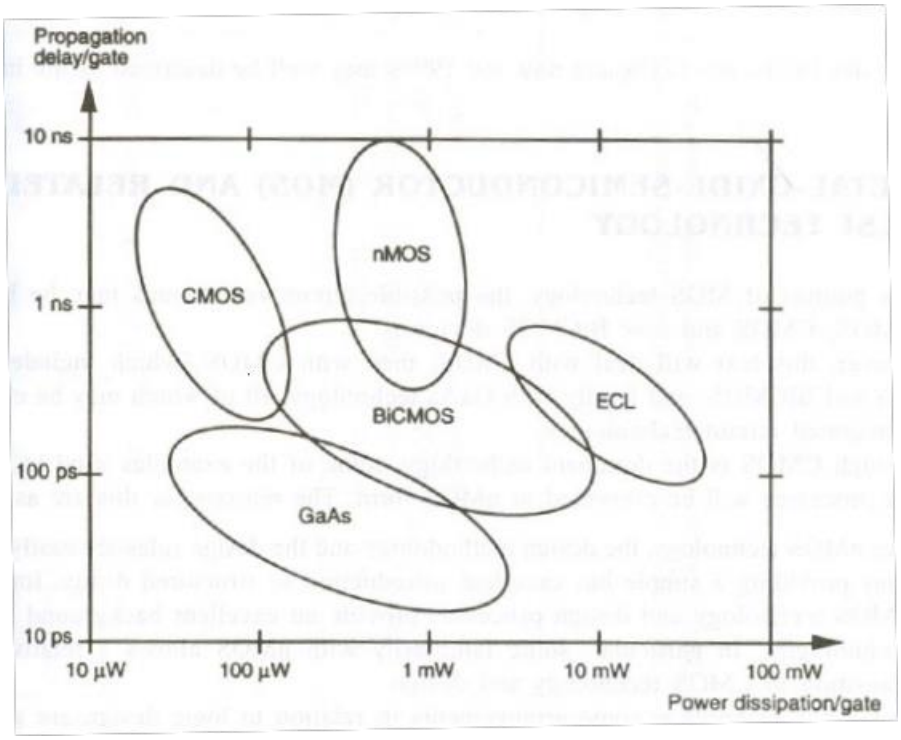


Figure 2.Comparison of available technologies

From the graph we can conclude that GaAs technology is better but still it is not used because of growing difficulties of GaAs crystal. CMOS looks to be a better option compared to nMOS since it consumes a lesser power. BiCMOS technology is also used in places where high driving capability is required and from the graph it confirms that, BiCMOS consumes more power compared to CMOS.

Basic MOS Transistors:

Why the name MOS?

We should first understand the fact that why the name Metal Oxide Semiconductor transistor, because the structure consists of a layer of Metal (gate), a layer of oxide (Sio2) and a layer of semiconductor. Figure 3 below clearly tell why the name MOS.

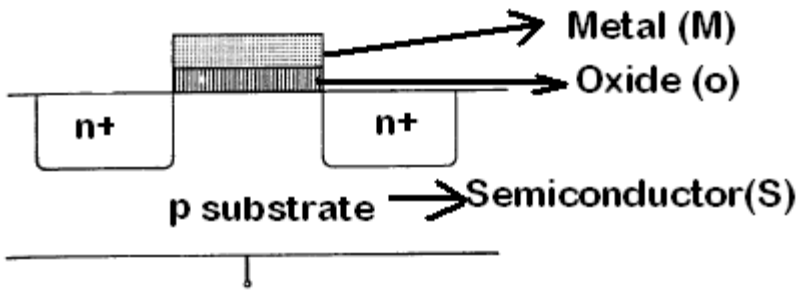


Figure 3. Cross Section of a MOS structure

We have two types of FETs. They are Enhancement mode and depletion mode transistor. Also we have PMOS and NMOS transistors.

In **Enhancement mode transistor** channel is going to form after giving a proper positive gate voltage. We have NMOS and PMOS enhancement transistors.

In **Depletion mode transistor** channel will be present by the implant. It can be removed by giving a proper negative gate voltage. We have NMOS and PMOS depletion mode transistors.

N-MOS enhancement mode transistor:-

This transistor is normally off. This can be made ON by giving a positive gate voltage. By giving a +ve gate voltage a channel of electrons is formed between source drain.

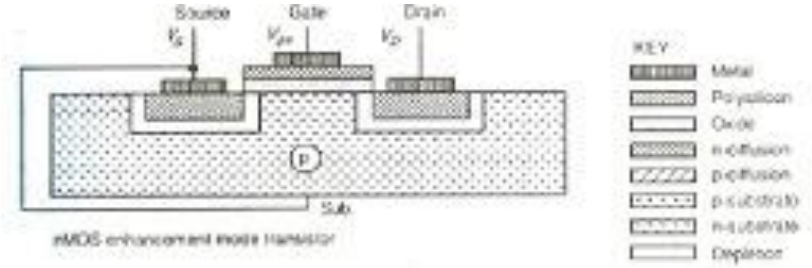


Fig 5. Nmos Enhancement transistor

P-MOS enhancement mode transistors:-

This is normally on. A Channel of Holes can be performed by giving a –ve gate voltage. In P-Mos current is carried by holes and in N-Mos its by electrons. Since the mobility is of holes less than that of electrons P-Mos is slower.

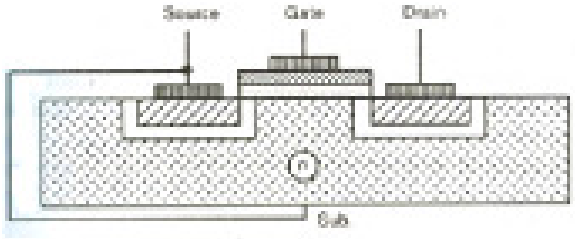


Fig 6. Pmos Enhancement transistor

N-MOS depletion mode transistor:-

This transistor is normally ON, even with Vgs=0. The channel will be implanted while fabricating, hence it is normally ON. To cause the channel to cease to exist, a –ve voltage must be applied between gate and source.

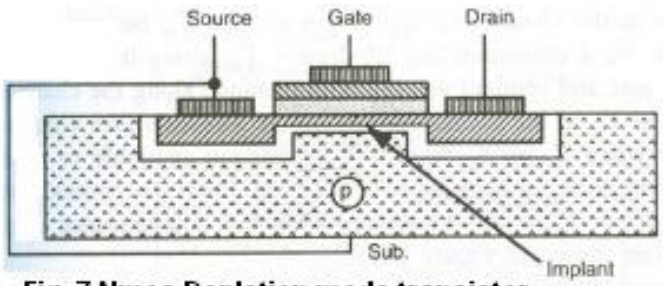


Fig. 7 Nmos Depletion mode transistor

NOTE: Mobility of electrons is 2.5 to 3 times faster than holes. Hence P-MOS devices will have more resistance compared to NMOS.

Enhancement mode Transistor action:-

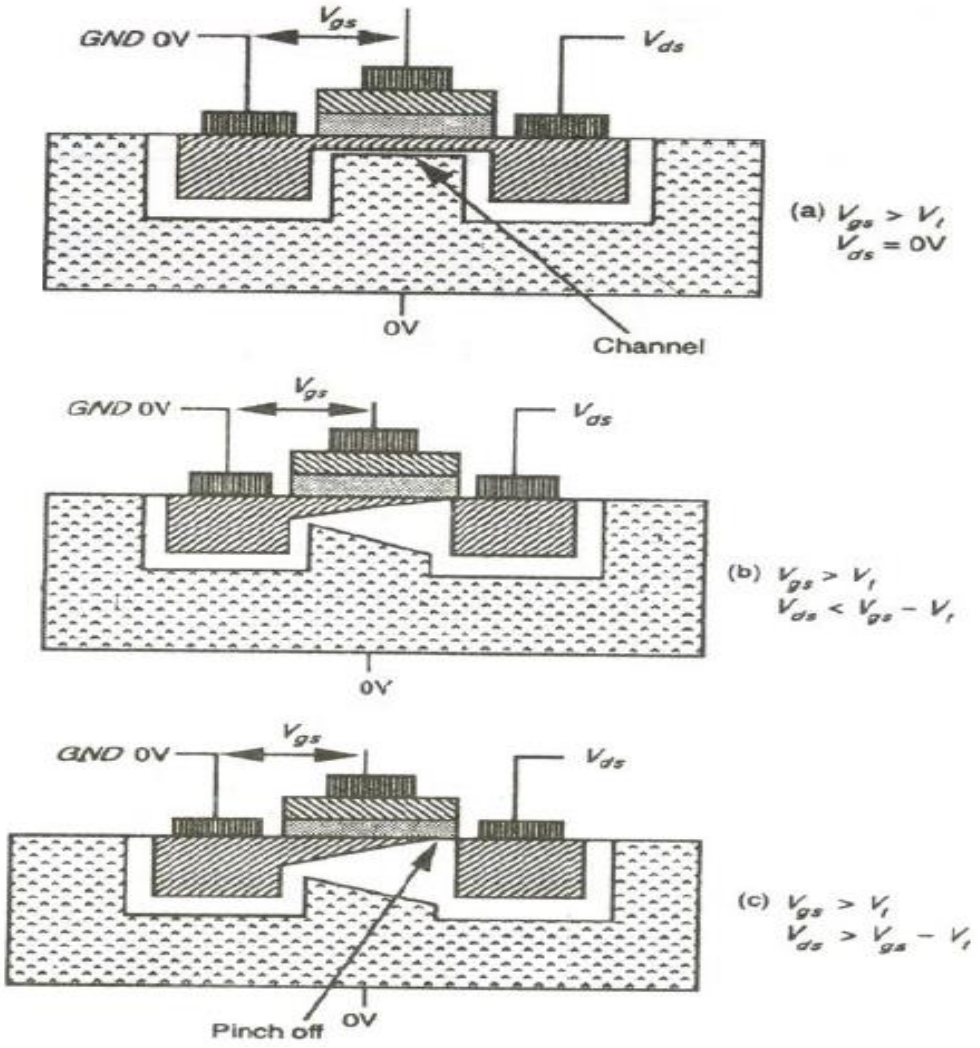


Figure5. (a)(b)(c) Enhancement mode transistor with different Vds Values

To establish the channel between the source and the drain a minimum voltage (Vt) must be applied between gate and source. This minimum voltage is called as ―Threshold Voltage. The complete working of enhancement mode transistor can be explained with the help of diagram a, b and c.

a) Vgs>Vt
   Vds = 0
   Since Vgs>Vt and Vds = 0 the channel is formed but no current flows between drain and source.

b) Vgs>Vt
   Vds<Vgs - Vt

This region is called the non-saturation Region or linear region where the drain current increases linearly with Vds. When Vds is increased the drain side becomes more reverse biased (hence more depletion region towards the drain end) and the channel starts to pinch. This is called as the pinch off point.

c) Vgs>Vt
   Vds>Vgs–Vt

This region is called Saturation Region where the drain current remains almost constant. As the drain voltage is increased further beyond (Vgs-Vt) the pinch off point starts to move from the drain end to the source end. Even if the Vds is increased more and more, the increased voltage gets dropped in the depletion region leading to a constant current. The typical threshold voltage for an enhancement mode transistor is given by Vt = 0.2 * Vdd.

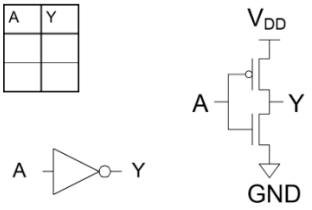
1.3.5 Depletion mode Transistor action: -

We can explain the working of depletion mode transistor in the same manner, as that of the enhancement mode transistor only difference is, channel is established due to the implant even when Vgs = 0 and the channel can be cut off by applying a -ve voltage between the gate and source. Threshold voltage of depletion mode transistor is around 0.8*Vdd.

CMOS Logic

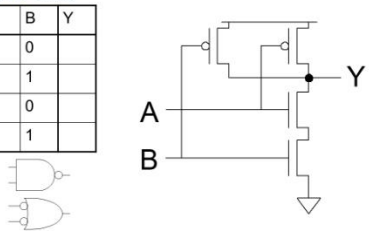
CMOS Inverter

A	Y



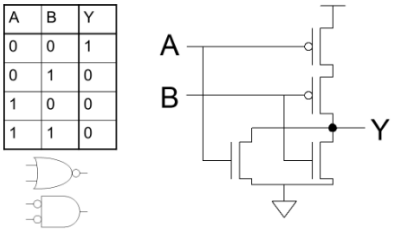
CMOS NAND Gate

A	B	Y
0	0	
0	1	
1	0	
1	1	



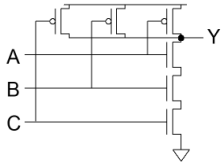
CMOS NOR Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

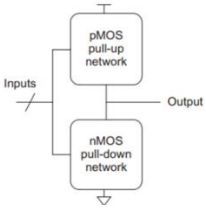


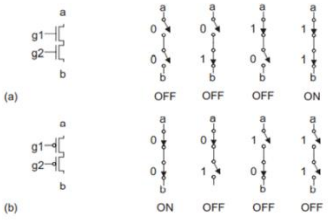
3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0



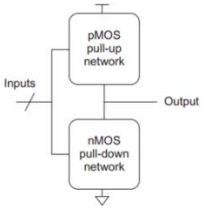
CMOS Logic Gates

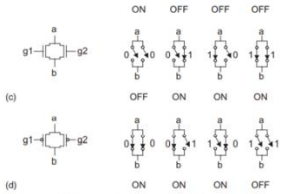




Connection behavior of Series and Parallel Transistors

CMOS Logic Gates

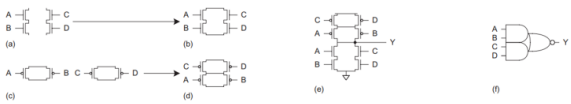




Connection behavior of Series and Parallel Transistors

Compound Gates

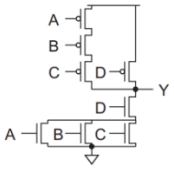
- Steps to build CMOS Circuit for Complex Expressions
  - A. Build nMOS Network from AOI or SOP Expression
    - a) And is implemented by series connections
    - b) OR s implemented by parallel connections
  - B. Build pMOS Network by applying DeMorgan's Principle to nMOS



CMOS compound gate for function $Y = \overline{(A.B) + (C.D)}$

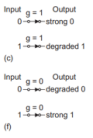
Exercise

- Sketch the static gate for the expression: $Y = \overline{(A + B + C).D}$



Pass Transistor

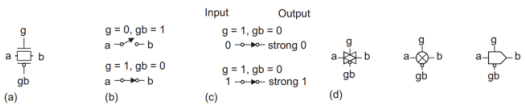
- Strength of a signal is measured by how closely it approximates an ideal voltage source.
- Stronger a signal, the more current it can source or sink.
- The power supplies, or rails, (VDD and GND) are the source of the strongest 1s and 0s.
- An nMOS transistor
  - perfect switch when passing a 0
  - imperfect at passing a 1
- A pMOS transistor
  - perfect switch when passing a 1
  - imperfect at passing a 0



"When an nMOS or pMOS is used alone as an imperfect switch, we call it a pass transistor."

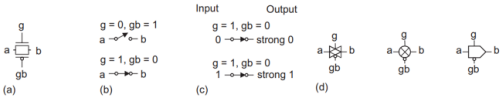
Transmission Gates

- By combining an nMOS and a pMOS transistor in parallel a switch when turned on passes both 0s and 1s in an acceptable fashion.
- This a transmission gate or pass gate.



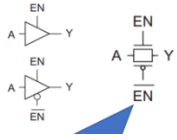
Transmission Gates

- Control and its complement are required to drive TG. (*Double Rail* Logic)
- So output is always strongly driven and the levels are never degraded. This is called a fully restored logic gate



Tristate Circuits – Tristate Buffer

EN / $\overline{EN}$	A	Y
0 / 1	0	Z
0 / 1	1	Z
1 / 0	0	0
1 / 0	1	1



MOS Transistor Theory

Introduction, Long-channel I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics (2.1, 2.2, 2.4 and 2.5 of TEXT2)

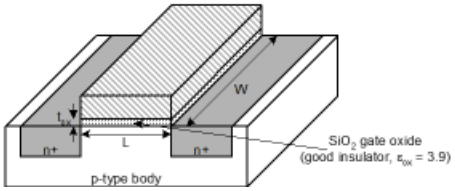
Long-Channel I-V Characteristics

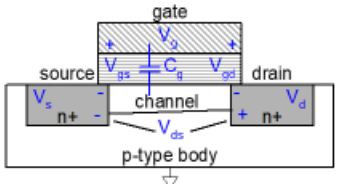
I-V Characteristics

- In Linear region, I_{ds} depends on
  - How much charge is in the channel?
  - How fast is the charge moving?

Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversions
  - Gate – oxide – channel
- $Q_{channel} = CV$
- $C = C_g = \varepsilon_{ox}WL/t_{ox} = C_{ox}WL$ where $C_{ox} = e_{ox} / t_{ox}$
- $V = V_{gc} - V_t = (V_{gs} - V_{ds}/2) - V_t$





Carrier velocity

- Charge is carried by e-
- Electrons are propelled by the lateral electric field between source and drain
  - $E = V_{ds}/L$
- Carrier velocity *v* proportional to lateral E-field
  - $v = \mu E$ μ called mobility
- Time for carrier to cross channel:
  - $t = L / v$

nMOS Linear I-V

- Now we know
  - How much charge $Q_{channel}$ is in the channel
  - How much time *t* each carrier takes to cross

$$I_{ds} = \frac{Q_{channel}}{t}$$
$$= \mu C_{ox} \frac{W}{L}\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds}$$
$$= \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} \qquad \beta = \mu C_{ox}\frac{W}{L}$$

nMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$I_{ds} = \beta\left(V_{gs} - V_t - V_{dsat}/2\right)V_{dsat}$$
$$= \frac{\beta}{2}\left(V_{gs} - V_t\right)^2$$

nMOS I-V Summary

- *Shockley* 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

Non-ideal I-V Effects

Mobility Degradation and Velocity Saturation

The carrier drift velocity, and hence current, is proportional to the lateral electric field $E_{lat} = V_{ds}/L$ between source and drain. The constant of proportionality is called the carrier mobility, R. The long-channel model assumed that carrier mobility is independent of the applied fields. This is a good approximation for low fields, but breaks down when strong lateral or vertical fields are applied.

A high voltage at the gate of the transistor attracts the carriers to the edge of the channel, causing collisions with the oxide interface that slow the carriers. This is called mobility degradation. Carriers approach a maximum velocity v_{sat} when high fields are applied. This phenomenon is called velocity saturation.

Mobility degradation can be modelled by replacing R with a smaller R_{eff} that is a function of V_{gs}. A universal model that matches experimental data from multiple processes reasonably well is

$$\mu_{\text{eff}-n} = \frac{540\frac{\text{cm}^2}{\text{V}\cdot\text{s}}}{1+\left(\frac{V_{gs}+V_t}{0.54\frac{\text{V}}{\text{nm}}t_{\text{ox}}}\right)^{1.85}} \qquad \mu_{\text{eff}-p} = \frac{185\frac{\text{cm}^2}{\text{V}\cdot\text{s}}}{1+\frac{\left|V_{gs}+1.5V_t\right|}{0.338\frac{\text{V}}{\text{nm}}t_{\text{ox}}}}$$

The α *-power law model* provides a simple approximation to capture this behavior. α is called the velocity saturation index and is determined by curve fitting measured I-V data. Transistors with long channels or low V_{DD} display quadratic I-V characteristics in saturation and are modeled with α = 2. As transistors become more velocity saturated, increasing V_{gs} has less effect on current and F decreases, reaching 1 for transistors that are completely velocity saturated. For simplicity, the model uses a straight line in the linear region. Overall, the model is based on three parameters that can be determined empirically from a curve fit of I-V characteristics: α, βP_c , and P_v.

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{Cutoff} \\ I_{\text{dsat}}\dfrac{V_{ds}}{V_{\text{dsat}}} & V_{ds} < V_{\text{dsat}} & \text{Linear} \\ I_{\text{dsat}} & V_{ds} > V_{\text{dsat}} & \text{Saturation} \end{cases}$$

Where,

$$I_{\text{dsat}} = P_c\frac{\beta}{2}V_{GT}^{\alpha}$$
$$V_{\text{dsat}} = P_v V_{GT}^{\alpha/2}$$

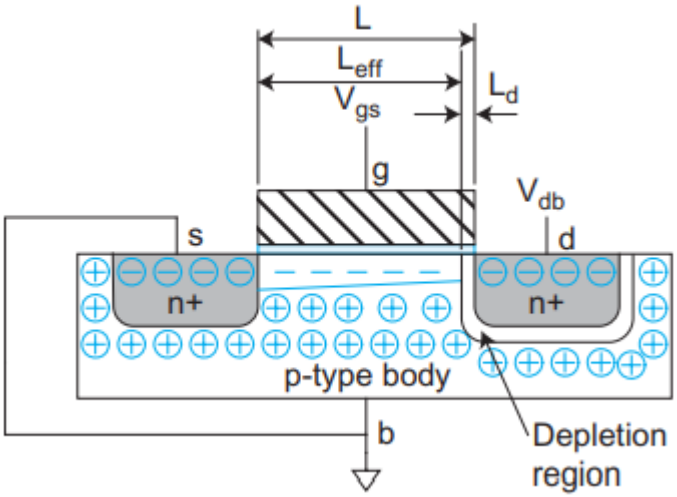
Channel Length Modulation

The depletion region effectively shortens the channel length to

$$L_{\text{eff}} = L - L_d$$

To avoid introducing the body voltage into our calculations, assume the source voltage is close to the body voltage so $Vdb \approx Vds$. Hence, increasing V_{ds} decreases the effective channel length. Shorter channel length results in higher current; thus, I_{ds} increases with V_{ds} in saturation. This can be crudely modelled by multiplying by a factor of $(1 + V_{ds}/V_A)$, where V_A is called the $Early\ voltage$. In the saturation region, we find

$$I_{ds} = \frac{\beta}{2} V_{\text{GT}}^2 \left(1 + \frac{V_{ds}}{V_A}\right)$$



Depletion region shortens effective channel length

Threshold Voltage Effects

Body Effect

When a voltage V_{sb} is applied between the source and body, it increases the amount of charge required to invert the channel, hence, it increases the threshold voltage. The threshold voltage can be modelled as

$$V_t = V_{t0} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right)$$

where V_{t0} is the threshold voltage when the source is at the body potential, Φ_s is the surface potential at threshold, and γ is the body effect coefficient, typically in the range 0.4 to $1V^{1/2}$.

In turn, these depend on the doping level in the channel, N_A.

The body effect further degrades the performance of pass transistors trying to pass the weak value (e.g., nMOS transistors passing a '1')

$$\phi_s = 2v_T \ln \frac{N_A}{n_i}$$

$$\gamma = \frac{t_{ox}}{\varepsilon_{ox}} \sqrt{2q\varepsilon_{si} N_A} = \frac{\sqrt{2q\varepsilon_{si} N_A}}{C_{ox}}$$

For small voltages applied to the source or body, EQ (2.35) can be linearized to

$$V_t = V_{t0} + k_\gamma V_{sb}$$

Where,

$$k_\gamma = \frac{\gamma}{2\sqrt{\phi_s}} = \frac{\sqrt{\frac{q\varepsilon_{si} N_A}{v_T \ln \frac{N_A}{n_i}}}}{2C_{ox}}$$

Drain-Induced Barrier Lowering The drain voltage V_{ds} creates an electric field that affects the threshold voltage. This drain-induced barrier lowering (DIBL) effect is seen more in short-channel transistors. It can be modelled as

$$V_t = V_{t0} - \eta V_{ds}$$

where η is the DIBL coefficient, typically on the order of 0.1 (often expressed as 100 mV/V).

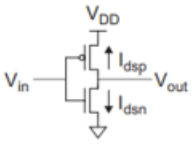
Drain-induced barrier lowering causes I_{ds} to increase with V_{ds} in saturation, in much the same way as channel length modulation does. This effect can be lumped into a smaller Early voltage V_A. More significantly, DIBL increases subthreshold leakage at high V_{ds}.

Short Channel Effect The threshold voltage typically increases with channel length. This phenomenon is especially pronounced for small L where the source and drain depletion regions extend into a significant portion of the channel, and hence is called the short channel effect or $V_t\ rolloff$. In some processes, a reverse short channel effect causes V_t to decrease with length.

There is also a narrow channel effect in which V_t varies with channel width; this effect tends to be less significant because the minimum width is greater than the minimum length.

DC Transfer Characteristics

Static CMOS Inverter DC Characteristics



	Cutoff	Linear	Saturated
nMOS	$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$	$V_{gsn} > V_{tn}$
	$V_{in} < V_{tn}$	$V_{in} > V_{tn}$	$V_{in} > V_{tn}$
		$V_{dsn} < V_{gsn} - V_{tn}$	$V_{dsn} > V_{gsn} - V_{tn}$
		$V_{out} < V_{in} - V_{tn}$	$V_{out} > V_{in} - V_{tn}$
pMOS	$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$	$V_{gsp} < V_{tp}$
	$V_{in} > V_{tp} + V_{DD}$	$V_{in} < V_{tp} + V_{DD}$	$V_{in} < V_{tp} + V_{DD}$
		$V_{dsp} > V_{gsp} - V_{tp}$	$V_{dsp} < V_{gsp} - V_{tp}$
		$V_{out} > V_{in} - V_{tp}$	$V_{out} < V_{in} - V_{tp}$

- V_{tn} - threshold voltage nMOS
- V_{tp} - threshold voltage pMOS

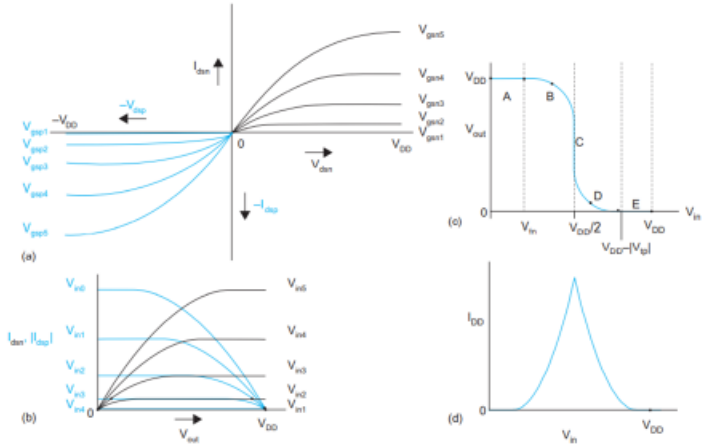
(V_{tp} is negative)

- Equations -in terms of V_{gs}/V_{ds} and Vin /Vout.
- Source of the nMOS transistor is grounded,

$V_{gsn} = V_{in}$ and $V_{dsn} = V_{out}$

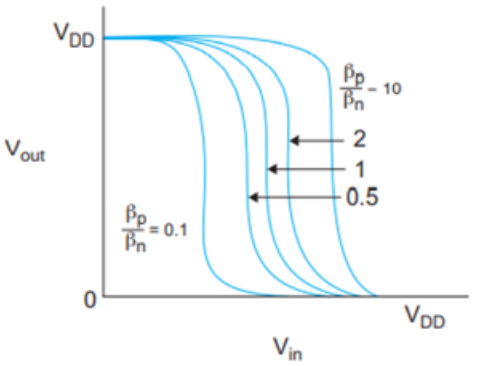
- As the source of the pMOS transistor is tied to VDD, Vgsp = Vin – VDD and Vdsp = Vout – VDD

Static CMOS Inverter DC Characteristics



Region	Condition	p-device	n-device	Output
A	$0 \le V_{in} < V_{tn}$	linear	cutoff	$V_{out} = V_{DD}$
B	$V_{tn} \le V_{in} < V_{DD}/2$	linear	saturated	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	saturated	saturated	V_{out} drops sharply
D	$V_{DD}/2 < V_{in} \le V_{DD} - \lvert V_{tp}\rvert$	saturated	linear	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} - \lvert V_{tp}\rvert$	cutoff	linear	$V_{out} = 0$

Beta Ratio Effects



- Inverters with different beta ratios

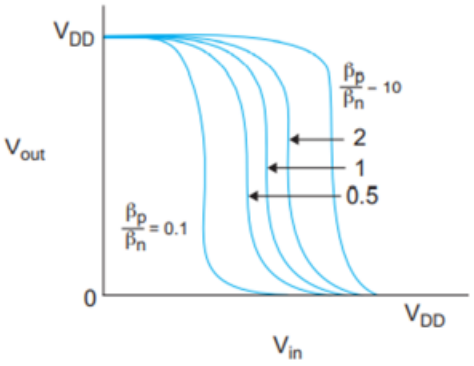
$$r = \beta_p / \beta_n$$

are called skewed inverters.

- If r > 1, the inverter is HI-skewed.
- If r < 1, the inverter is LO-skewed.
- If r = 1, the inverter has normal skew or is unskewed.

Beta Ratio Effects

Beta Ratio Effects



- HI-skew inverter - stronger pMOS transistor.
- Input is VDD /2
- Output greater VDD /2.
- Input threshold must be higher than an unskewed inverter.
- LO-skew inverter has a weaker pMOS transistor - Lower switching threshold.

Beta Ratio Effects

- The inverter threshold can also be computed analytically.

From the long-channel models of for saturated transistors:

$$I_{dn} = \frac{\beta_n}{2}(V_{inv} - V_{tn})^2$$

$$I_{dp} = \frac{\beta_p}{2}(V_{inv} - V_{DD} - V_{tp})^2$$

By setting the currents to be equal and opposite, we can solve for V_{inv} as a function of r:

$$V_{inv} = \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{\frac{1}{r}}}{1 + \sqrt{\frac{1}{r}}}$$

Beta Ratio Effects

- In the limit that the transistors are fully velocity saturated

$$I_{dn} = W_n C_{ox} v_{sat-n}(V_{inv} - V_{tn})$$
$$I_{dp} = W_p C_{ox} v_{sat-p}(V_{inv} - V_{DD} - V_{tp})$$

- Redefining $r = W_p v_{sat-p} / W_n v_{sat-n}$, the inverter threshold

$$V_{inv} = \frac{V_{DD} + V_{tp} + V_{tn}\frac{1}{r}}{1 + \frac{1}{r}}$$

- In either case, if $V_{tn} = -V_{tp}$ and r = 1, $V_{inv} = V_{DD}/2$ as expected.
- Velocity saturated inverters are more sensitive to skewing because their DC transfer characteristics are not as sharp.

Noise Margin

Noise Margin

- Noise margin allows to determine the allowable noise voltage on the input of a gate so that the output will not be corrupted.
- Noise margin (or noise immunity) uses two parameters:
  - the LOW noise margin, NM_L
  - the HIGH noise margin, NM_H.
- NM_L is defined as difference in maximum LOW input voltage recognized by the receiving gate and the maximum LOW output voltage produced by the driving gate.

$$NM_L = V_{IL} - V_{OL}$$

Noise Margin

- The value of NMH is the difference between the minimum HIGH output voltage of the driving gate and the minimum HIGH input voltage recognized by the receiving gate. Thus,

$$NM_H = V_{OH} - V_{IH}$$

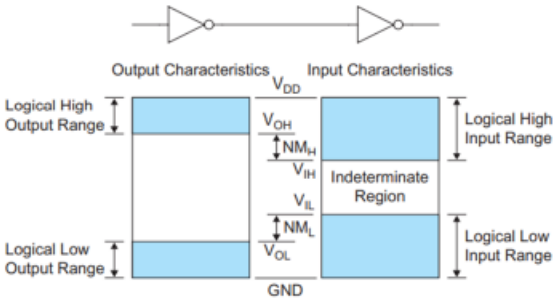
Where,

V_{IH} = minimum HIGH input voltage

V_{IL} = maximum LOW input voltage

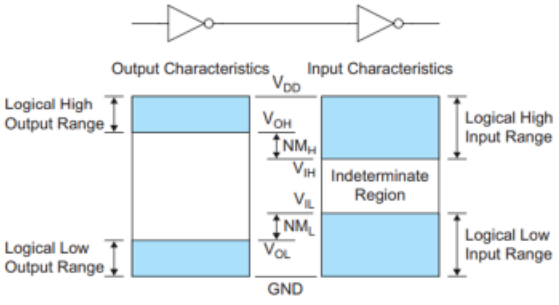
V_{OH}= minimum HIGH output voltage

V_{OL} = maximum LOW output voltage



Noise Margin

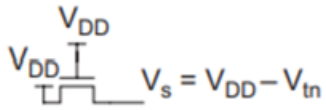
- Inputs between VIL and VIH are said to be in the indeterminate region or forbidden zone and do not represent legal digital logic levels.
- Therefore, it is generally desirable to have VIH as close as possible to VIL and for this value to be midway in the "logic swing," VOL to VOH.



Pass Transistor DC Characteristics

Pass Transistor DC Characteristics

- Figure shows an nMOS transistor with the gate and drain tied to VDD.
- If the source is initially at $V_s = 0$.
- $V_{gs} > V_{tn}$, so the transistor is ON and current flows.
- If the voltage on the source rises to $V_s = V_{DD} - V_{tn}$, V_{gs} falls to V_{tn} and the transistor cuts itself OFF.
- Therefore, nMOS transistors attempting to pass a 1 never pull the source above VDD – Vtn.
- This loss is sometimes called a threshold drop.



Pass Transistor DC Characteristics

- pMOS transistors pass 1s well but 0s poorly.
- If the pMOS source drops below $|V_{tp}|$, the transistor cuts off.
- Hence, pMOS transistors only pull down to within a threshold above GND, as shown in Figure